

Power MOSFET, 40 A


SOT-227

PRODUCT SUMMARY	
V_{DSS}	500 V
$R_{DS(on)}$ (typical)	0.084 Ω
I_D	40 A
Type	Modules - MOSFET
Package	SOT-227

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Low $R_{DS(on)}$
- Fully insulated package
- UL pending
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level


RoHS
COMPLIANT

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain current, V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	40	A
		$T_C = 100\text{ }^\circ\text{C}$	26	
Pulsed drain current	$I_{DM}^{(1)}$		160	
Power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	430	W
Linear derating factor			3.45	W/ $^\circ\text{C}$
Gate to source voltage	V_{GS}		± 30	V
Peak diode recovery dV/dt	$dV/dt^{(2)}$		9.0	V/ns
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	$^\circ\text{C}$

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 (2) $I_{SD} \leq 40\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150\text{ }^\circ\text{C}$

AVALANCHE CHARACTERISTICS				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Single pulse avalanche energy	$E_{AS}^{(1)}$	-	1240	mJ
Avalanche current	$I_{AR}^{(2)}$	-	40	A
Repetitive avalanche energy	$E_{AR}^{(2)}$	-	43	mJ

Notes

- (1) Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.55\text{ mH}$, $R_G = 25\text{ }^\circ\Omega$, $I_{AS} = 40\text{ A}$, $dV/dt = 5.5\text{ V/ns}$ (see fig. 12a)
 (2) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)



THERMAL RESISTANCE				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Junction to case	R_{thJC}	-	0.29	°C/W
Case to sink, flat, greased surface	R_{thCS}	0.05	-	

STATIC CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.60	-	V/°C
Static drain to source on-resistance	$R_{DS(on)}^{(1)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$	-	0.084	0.10	Ω
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Drain to source leakage current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	μA
Gate to source forward leakage	I_{GSS}	$V_{GS} = 30\text{ V}$	-	-	250	
Gate to source reverse leakage		$V_{GS} = -30\text{ V}$	-	-	-250	nA

Note

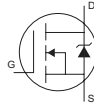
(1) Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

DYNAMIC CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 28\text{ A}$	23	-	-	S	
Total gate charge	$Q_g^{(1)}$	$I_D = 40\text{ A}$ $V_{DS} = 400\text{ V}$ $V_{GS} = 10\text{ V}$; see fig. 6 and 13	-	-	270	nC	
Gate to source charge	$Q_{gs}^{(1)}$		-	-	84		
Gate to drain ("Miller") charge	$Q_{gd}^{(1)}$		-	-	130		
Turn-on delay time	$t_{d(on)}^{(1)}$	$V_{DD} = 250\text{ V}$ $I_D = 40\text{ A}$ $R_g = 1.0\text{ }\Omega$ $V_{GS} = 10\text{ V}$, see fig. 10	-	25	-	ns	
Rise time	$t_r^{(1)}$		-	140	-		
Turn-off delay time	$t_{d(off)}^{(1)}$		-	55	-		
Fall time	$t_f^{(1)}$		-	74	-		
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5	-	8310	-	pF	
Output capacitance	C_{oss}		-	960	-		
Reverse transfer capacitance	C_{rss}		-	120	-		
Output capacitance	C_{oss}		$V_{GS} = 0\text{ V}, V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	10 170		-
			$V_{GS} = 0\text{ V}, V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	240		-
Effective output capacitance	$C_{oss\text{ eff.}}^{(2)}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to }480\text{ V}$	-	440	-		

Notes

(1) Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

(2) $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DSS}

DIODE CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	40	A
Pulsed source current (body diode)	$I_{SM}^{(1)}$		-	-	160	
Diode forward voltage	$V_{SD}^{(2)}$	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 40\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1	V
Reverse recovery time	$t_{rr}^{(2)}$	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 47\text{ A}$; $dI/dt = 100\text{ A}/\mu\text{s}$	-	620	940	ns
Reverse recovery charge	Q_{rr}		-	14	21	μC
Reverse recovery current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$	-	38	-	A
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- (2) Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

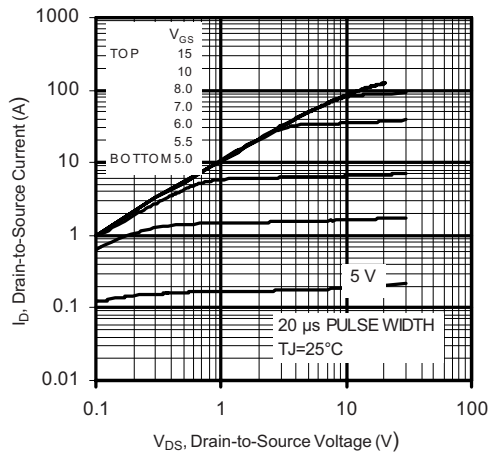


Fig. 1 - Typical Output Characteristics

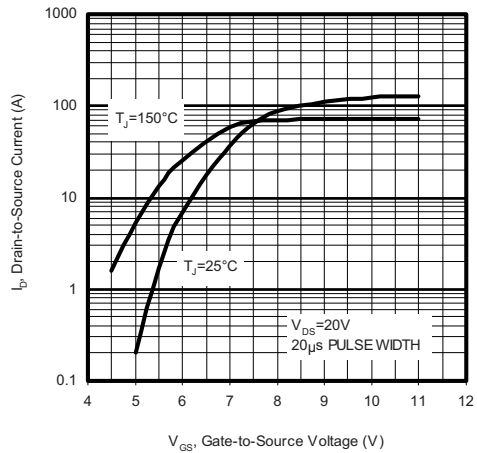


Fig. 3 - Typical Transfer Characteristics

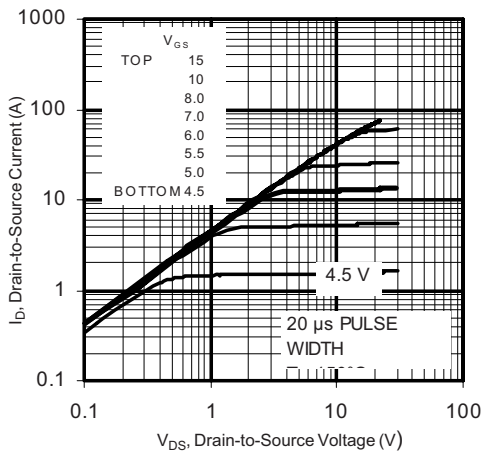


Fig. 2 - Typical Output Characteristics

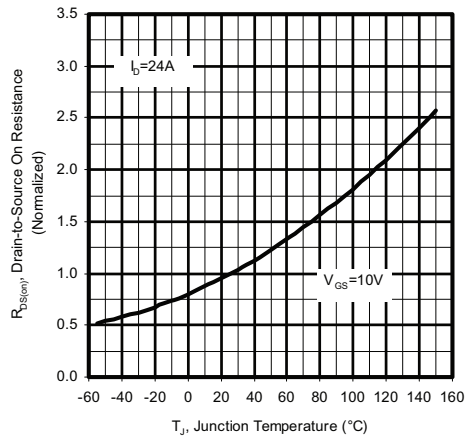


Fig. 4 - Normalized On-Resistance vs. Temperature

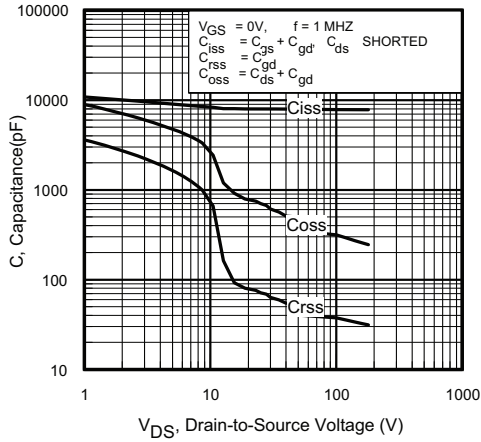


Fig. 5 - Typical Capacitance vs. Drain to Source Voltage

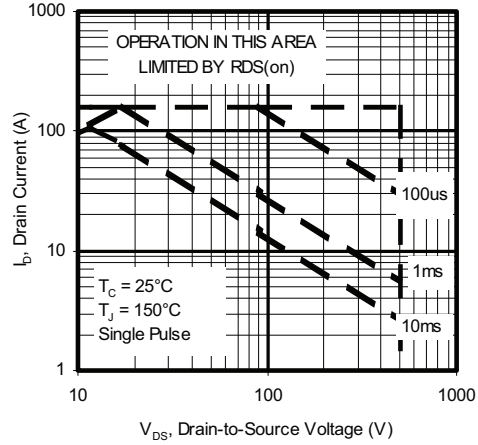


Fig. 8 - Maximum Safe Operating Area

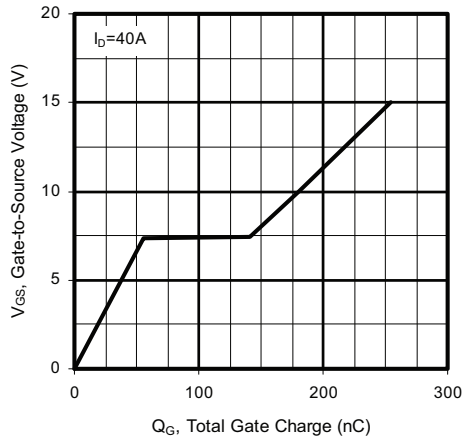


Fig. 6 - Typical Gate Charge vs. Gate to Source Voltage

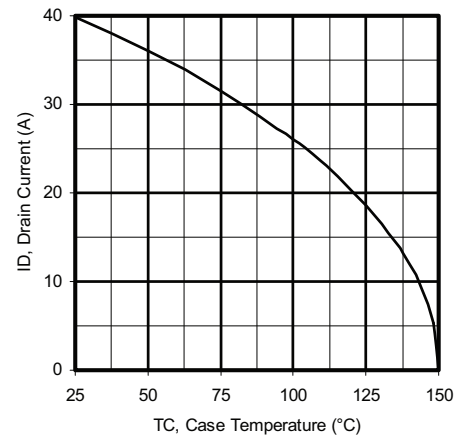


Fig. 9 - Maximum Drain Current vs. Case Temperature

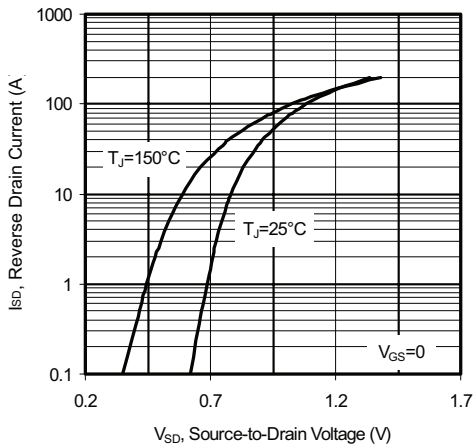


Fig. 7 - Typical Source Drain Diode Forward Voltage

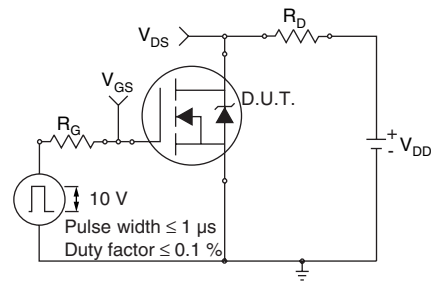


Fig. 10a - Switching Time Test Circuit

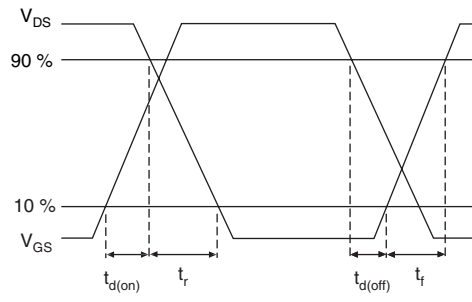


Fig. 10b - Switching Time Waveforms

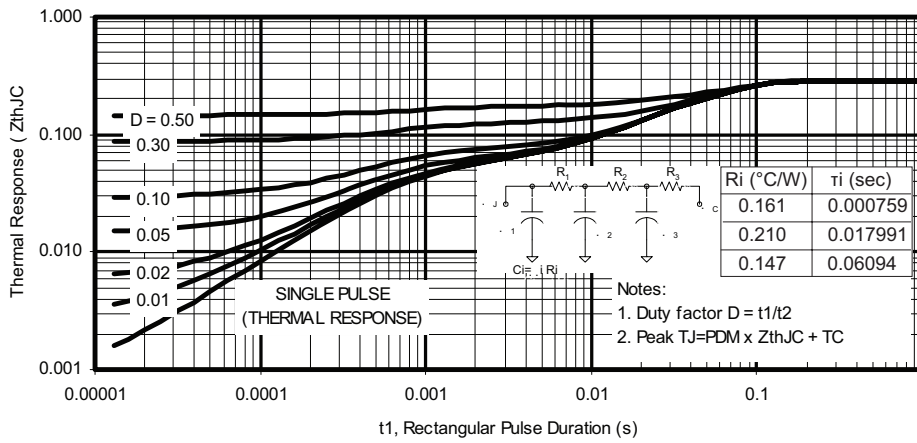


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction to Case

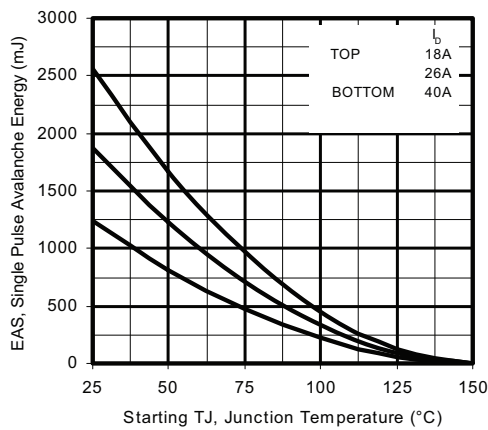


Fig. 12a - Maximum Avalanche Energy vs. Drain Current

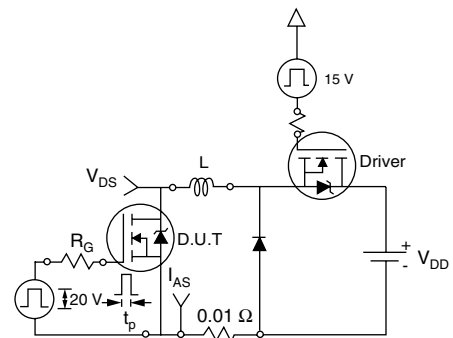


Fig. 12b - Unclamped Inductive Test Circuit

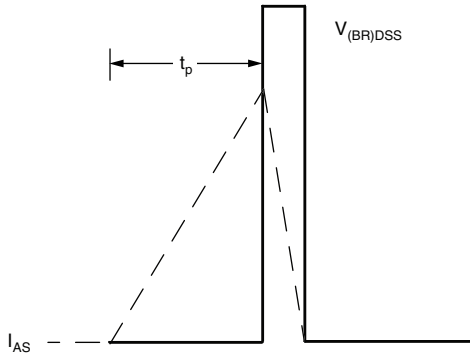


Fig. 12c - Unclamped Inductive Waveforms

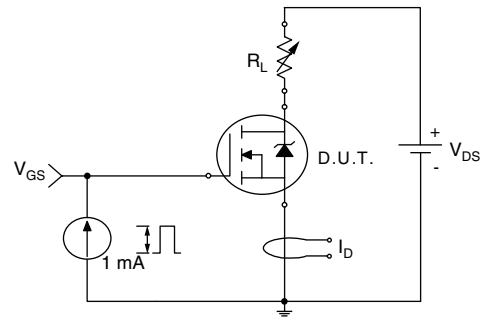


Fig. 13a - Gate Charge Test Circuit

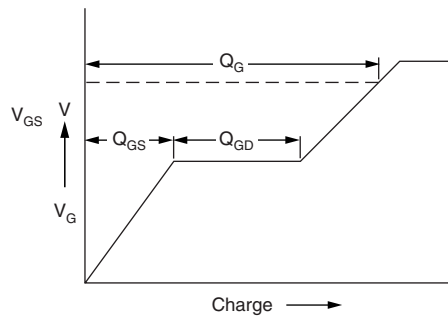


Fig. 13b - Basic Gate Charge Waveform

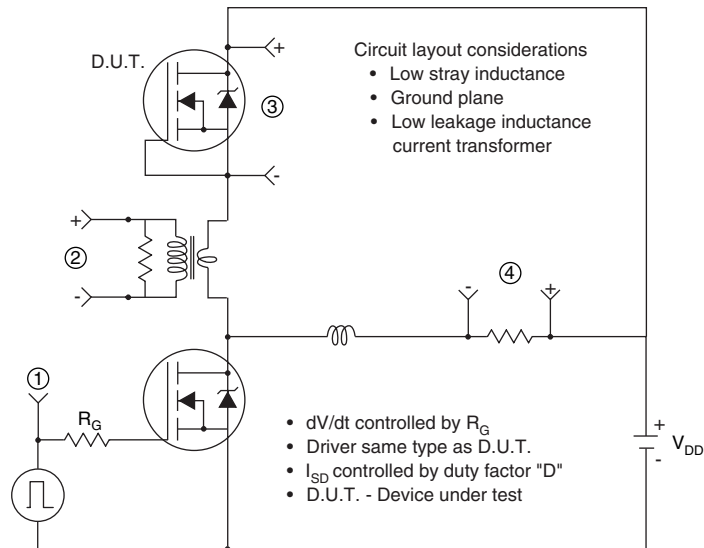
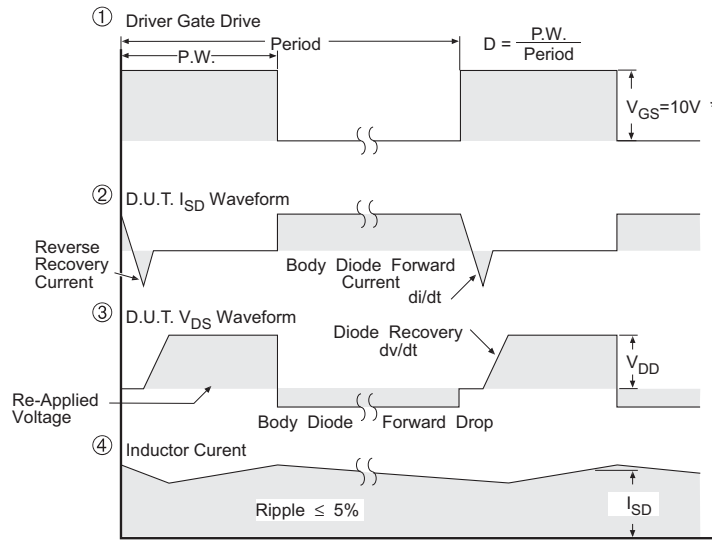


Fig. 13c - Peak Diode Recovery dV/dt Test Circuit



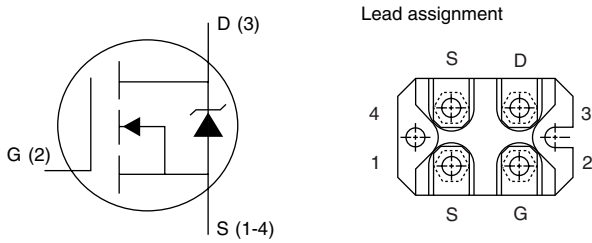
* $V_{GS} = 5V$ for Logic Level Devices

Fig. 14 - For N-Channel Power MOSFETs

ORDERING INFORMATION TABLE

Device code	F	C	40	S	A	50	FK	P
	①	②	③	④	⑤	⑥	⑦	⑧

- ① - Power MOSFET
- ② - Generation 6.2/6.3 MOSFET silicon DBC construction
- ③ - Current rating (40 = 40 A)
- ④ - Single switch (see Circuit Configuration table)
- ⑤ - SOT-227
- ⑥ - Voltage rating (50 = 500 V)
- ⑦ - MOSFET K speed
- ⑧ -
 - None = Standard production
 - P = Lead (Pb)-free

CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Single switch no diode	S	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95036
Packaging information	www.vishay.com/doc?95037



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